FIGS. 3 (a) to (e) are schematic diagrams of the plating growing process for illustrating the effect of the present invention;

FIGS. 4 (a) to (e) are sectional process diagrams showing the procedures of the damascene process according to an embodiment of the present invention;

FIGS. 5 (a) and (b) are experimental data diagrams that compare the Rs of the Damascene wiring formed in an embodiment of the present invention to the Rs of the damascene wiring according to a prior art;

FIGS. 6 (a) to (c) are sectional process diagrams showing the procedures of a conventional damascene process; and

FIGS. 7 (a) to (c) are schematic diagrams for illustrating the effect of the additive in the plating bath used in the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Next, the embodiments of a semiconductor device according to the present invention will be described referring to the drawings. In the Cu plating process in the damascene process, as shown in the conventional example, bottom-up plating using a plating bath containing a brightener and a suppressor is required to bury fine patterns without forming voids; however, protrusions occur on the fine patterns. As described above, this is caused by the concentration gradient of the brightener 16 for accelerating the plating reaction. In order to inhibit the protrusions on the wiring patterns, it is considered that